**Individual Estimated Cell Height**

Across all cells, there are fixed extra lengths that are to be added to pull-up and pull-down network lengths which are needed for contacts, contact spacing, well padding, etc. According to the example document:

Extra length =

**1. Inverter**

The smallest inverter is designed with the nMOS channel width of , and the pMOS channel width equal

The table below shows estimations for each inverter cell’s layout height taking into account folded cells.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cell** | **Folding Factor** | **Pull-up Height** | **Pull-down Height** | **Layout Height** |
| **Inv1x1** | **0** | **4** | **10** | **42** |
| **Inv1x2** | **0** | **8** | **19** | **55** |
| **Inv1x4** | **0** | **16** | **38** | **82** |
| **Inv1x8** | **x1** | **16 (folded)** | **38 (folded)** | **82** |

**2. Tristate Inverter**

The smallest tristate inverter is sized such that the nMOS channel width is equal , and the pMOS channel width equal in order to have the same equivalent resistance of the smallest inverter.

The table below shows estimations for each tristate inverter cell’s layout height taking into account folded cells.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cell** | **Folding Factor** | **Pull-up Height** | **Pull-down Height** | **Layout Height** |
| **Tri\_Inv1x1** | **0** | **8** | **19** | **55** |
| **Tri\_Inv1x2** | **0** | **16** | **38** | **82** |
| **Tri\_Inv1x4** | **x1** |  |  | **82** |
| **Tri\_Inv1x8** | **x2** |  |  | **100** |

**3. 2-input NAND Gate**

The smallest 2-input NAND gate is sized such that the nMOS channel width is equal , and the pMOS channel width equal in order to have the same equivalent resistance of the smallest inverter.

The table below shows estimations for each 2-input NAND cell’s layout.

|  |  |  |  |
| --- | --- | --- | --- |
| **Cell** | **Pull-up Height** | **Pull-down Height** | **Layout Height** |
| **NAND2x1** |  | **8** | **46** |
| **NAND2x2** | **19.219** | **16** | **63** |
| **NAND2x4** | **38.438** | **32** | **98** |

**4. 2-input NOR Gate**

The smallest 2-input NOR gate is sized such that the nMOS channel width is equal , and the pMOS channel width equal in order to have the same equivalent resistance of the smallest inverter.

The table below shows estimations for each 2-input NOR cell’s layout.

|  |  |  |  |
| --- | --- | --- | --- |
| **Cell** | **Pull-up Height** | **Pull-down Height** | **Layout Height** |
| **NOR2x1** |  | **4** | **51** |
| **NOR2x2** | **38.4 38** | **8** | **74** |
| **NOR2x4** | **76.8 77** | **16** | **121** |

**5. The Complex Gate f(x,y,z,w) =**

The smallest AOI22 cell is sized such that the nMOS channel width is equal to , and the pMOS channel width equal in order to have the same equivalent resistance of the smallest inverter.

The table below shows estimations for each AOI22 cell’s layout.

|  |  |  |  |
| --- | --- | --- | --- |
| **Cell** | **Pull-up Height** | **Pull-down Height** | **Layout Height** |
| **AOI22x1** | **8** | **19** | **55** |
| **AOI22x2** | **16** | **38** | **82** |