**Individual Estimated Cell Height**

Across all cells, there are fixed extra lengths that are to be added to pull-up and pull-down network lengths which are needed for contacts, contact spacing, well padding, etc. According to the example document:

Extra length =

**1. Inverter**

The smallest inverter is designed with the nMOS channel width of , and the pMOS channel width equal

The table below shows estimations for each inverter cell’s layout height taking into account folded cells.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cell** | **Folding Factor** | **Pull-up Height** | **Pull-down Height** | **Layout Height** |
| **Inv1x1** | **0** | **4** | **10** | **42** |
| **Inv1x2** | **0** | **8** | **19** |  |
| **Inv1x4** | **0** | **16** | **38** | **82** |
| **Inv1x8** | **1 times** | **16 (folded)** | **38 (folded)** |  |